



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,119	05/05/2005	Hassan Ihs	SC12161ET	2446

23125 7590 11/14/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER

NGUYEN, LINH V

ART UNIT PAPER NUMBER

2819

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8A

Office Action Summary	Application No. 10/534,119	Applicant(s) IHS ET AL.	
	Examiner Linh V. Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/505</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to communication filed on 10/534119 filed on 05/05/05. Claims 1 – 18 are pending on this application.

Information Disclosure Statement

2. The reference "2001/038350" of the IDS filed 5/5/05 does not disclose any information relating to the invention. It seems there is an error to the number of this reference.

Specification

3. A Cross-reference to Related Applications for PCT continuation data needs to be adding into the first paragraph of specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 5, 11, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakimura Pub.No.: 2002/0175846.

Regarding claim 1, Fig. 5 of Sakimura discloses a continuous time sigma delta converter (Fig. 5) comprising: conversion means (Fig. 5) having known non-ideal characteristics (Fig. 4) and arranged to provide an output signal (output of 5); a compensation circuit comprising error modeling components (6, 8a, 12,20) arranged to substantially model the non-ideal characteristics of the conversion means (output of 5); and summation means (10, 10b, 10c) coupled to combine the compensation signal (11ma, 11b, 12b) with the output signal (output of 5) in order to provide a compensated output signal (Yz).

Regarding claim 2, Fig. 5 further comprises the summation means (10c) being arranged to subtract the compensation signal (12) from the output signal (output of 5) in order to provide the compensated output signal (Yz).

Regarding claim 3, Fig. 5 of Sakimura disclose a compensation circuit (20, 12, 8a, 6) for use with a continuous time sigma delta converter (Fig. 5) having known non-ideal characteristics (Fig. 4), the compensation circuit comprising error modeling components (6, 8a, 20, 12) arranged to substantially model the non-ideal characteristics (output of 5) of the converter (Fig. 5) in order to provide a compensation signal (12, 11) wherein the compensation signal is combinable (10) with a non-ideal output of the converter (output of 5) in order to provide a compensated output signal (Yz).

Regarding claim 4, Fig. 5 discloses a method for compensating for known non-ideal characteristics (Fig. 4) in a continuous time sigma delta converter (Fig. 5), the

Art Unit: 2819

method comprising: converting an input signal of one time domain (X_z) to an output signal of another time domain using a converter (4, 5) having known non-ideal characteristics (Fig. 4); modeling the non-ideal characteristics of the converter in a compensation circuit (20, 12); combining (10) a compensation signal output (11, 12) with the output signal of the converter (4, 5) in order to provide a compensated output signal (Y_z).

Regarding claim 5, Fig. 5 comprises the non-ideal characteristics (output of 5) being associated with a feedback path (6, 8a) of the converter.

Regarding claim 11, Fig. 5 further comprises the non-ideal characteristics being associated with a feedback path (6, 8a) of the converter.

Regarding claim 12 further comprises the non-ideal characteristics being associated with a feedback path (6, 8a) of the converter.

6. Claims 1, 3, 4, 8 – 10, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Handel et al. U.S. Patent No. 6,407,685.

Regarding claim 1, Fig. 4 [A, B, C] of Handel et al. discloses a continuous time sigma delta converter (310; Col. 5 lines 47) comprising: conversion means (310) having known non-ideal characteristics (Table 4 on Col. 19) and arranged to provide an output signal (X_k); a compensation circuit (340) comprising error modeling components (460, 455, 485, 490, 495) arranged to substantially model the non-ideal characteristics of the conversion means (X_k); and summation means (350, 490) coupled to combine the

compensation signal (S_i) with the output signal (X_k) in order to provide a compensated output signal (Y_k).

Regarding claim 3, Fig. 4 [A, B, C] of Handel et al. disclose a compensation circuit (340) for use with a continuous time sigma delta converter (310; Col. 5 lines 47) having known non-ideal characteristics (Table 4 on Col. 19), the compensation circuit comprising error modeling components (320) arranged to substantially model the non-ideal characteristics of the converter (X_k) in order to provide a compensation signal (S_i) wherein the compensation signal is combinable (490, 350) with a non-ideal output of the converter (X_k , Y_k) in order to provide a compensated output signal (Y_k).

Regarding claim 4, Fig. 4 [A, B, C] of Handel et al. disclose a method for compensating for known non-ideal characteristics (Table 4 on Col. 19) in a continuous time sigma delta converter (310; Col. 5 lines 47), the method comprising: converting an input signal of one time domain (S_t) to an output signal of another time domain (X_k) using a converter (310) having known non-ideal characteristics (Table 4 on Col. 19); modeling the non-ideal characteristics of the converter in a compensation circuit (340); combining (490, 350) a compensation signal output (S_i) with the output signal (X_k) of the converter (310) in order to provide a compensated output signal (Y_k).

Regarding claims 8, 17, and 18 wherein the compensation circuit (320) having calibration parameters (460) determined by a dichotomy technique which iteratively refines the values of the calibration parameters (Fig. 5, 12).

Regarding claim 9, Fig. 5 of Handel et al. discloses a method for producing calibration parameters for use in the compensation circuit (Fig. 4A) the method

Art Unit: 2819

comprising the steps of: collecting output samples from the converter (Fig. 4B, 4C); calculating a Signal to Noise and Distortion Ratio of the collected data (equation 6 on Col. 11); determining whether the calculated Signal to Noise and Distortion Ratio (Fig. 5 meets specified performance criteria; selectively recalculating the Signal to Noise and Distortion Ratio in dependence upon the step of determining, using a calibration algorithm (Fig. 5).

Regarding claim 10, wherein the calibration algorithm uses a dichotomy technique, which iteratively refines the values of the calibration parameters (Fig. 5, 12).

7. Claims 6 – 7, and 13 - 16 rejected under 35 U.S.C. 102 (a) as anticipated over Handel et al. as applied to claims 1, 3, and 4 above, and in view of Applicant Admitted Prior Art (AAPA).

Sigma-Delta converter of Handel et al. of as applied to claims 1, 3 and 4 above, does not explicitly disclose the non-ideal characteristics including asymmetrical or symmetrical errors associated with non-ideal rising and falling edges of signal transitions of the converter. However the non-ideal of asymmetrical or symmetrical errors associated with non-ideal rising and falling edges of signal transition of the converter is an intrinsic characteristic by the feedback path of sigma-delta converter (See under Background of AAPA, on page 3, lines 5 – 20).

Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

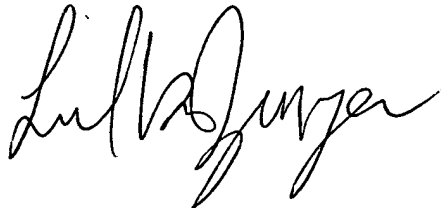
Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

11/9/05

Linh Van Nguyen

Art Unit 2819

A handwritten signature in black ink, appearing to read 'Linh Van Nguyen', is written over the typed name.